



LC320WUG

Product Specification

SPECIFICATION FOR APPROVAL

() Preliminary Specification

(●) Final Specification

Title	32.0" WUXGA TFT LCD
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BUYER	General
MODEL	

SUPPLIER	LG.Display Co., Ltd.
*MODEL	LC320WUG
SUFFIX	SCA1 (RoHS Verified)

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE	DATE
/		
/		
/		

Please return 1 copy for your confirmation with
your signature and comments.

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TV Products Development Dept.
LG. Display LCD Co., Ltd

Ver. 1.0



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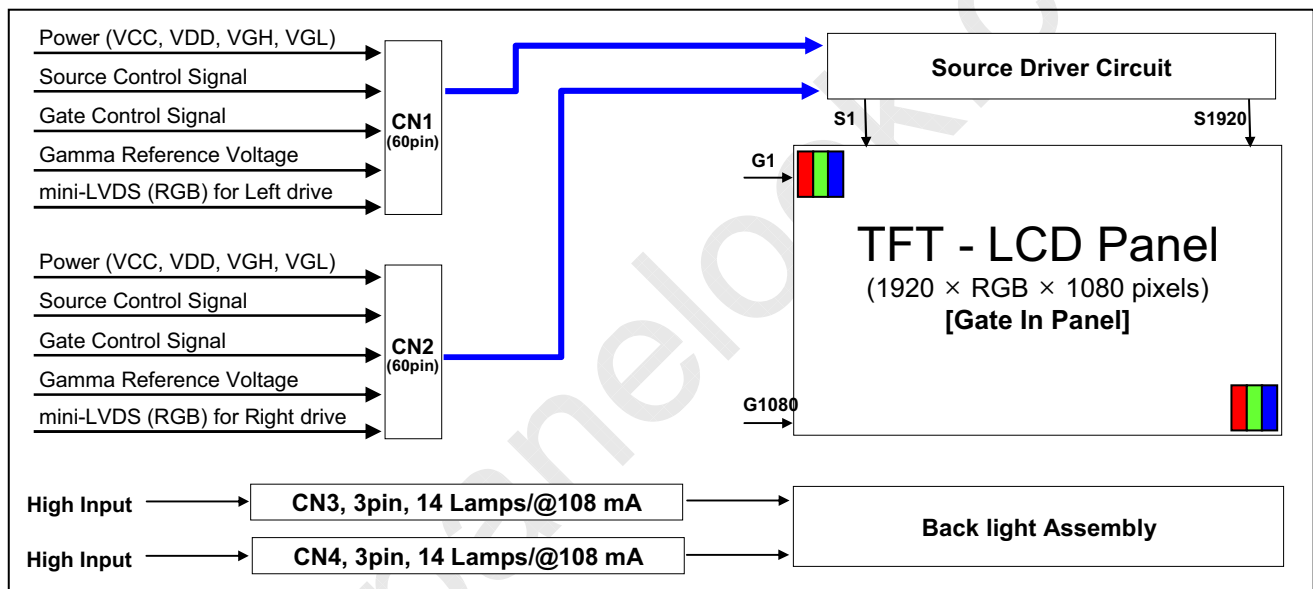
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1. General Description

The LC320WUG is a Color Active Matrix Liquid Crystal Display with an integral External Electrode Fluorescent Lamp(EEFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 31.55 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.

It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	31.55 inches(801.31mm) diagonal
Outline Dimension	760.0(H) x 450.0 (V) x 32.5 mm(D) (Typ.)
Pixel Pitch	0.36375 mm x 0.36375 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors (※ 1.06B colors @ 10 bit (D) System Output)
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals Gate D-IC : Gate In Panel
Luminance, White	1500 nit (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total180W
Weight	5.0Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%)

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2. Absolute Maximum Ratings

The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

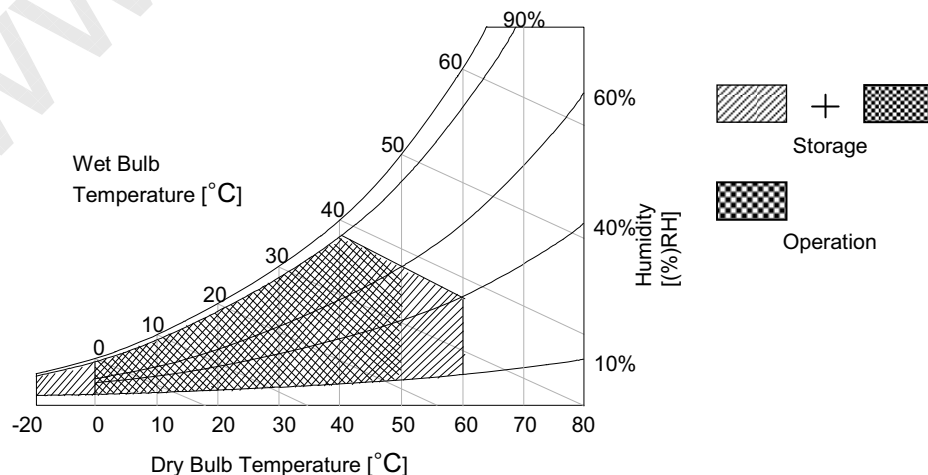
Parameter	Symbol	Value		Unit	Note
		Min	Max		
Logic Power Voltage	VCC	-0.5	+4.0	V _{DC}	1
Gate High Voltage	VGH	+18.0	+30.0	V _{DC}	
Gate Low Voltage	VGL	-8.0	-4.0	V _{DC}	
Source D-IC Analog Voltage	VDD	-0.3	+18.0	V _{DC}	
Gamma Ref. Voltage (Upper)	VGMH	$\frac{1}{2}VDD-0.5$	$VDD+0.5$	V _{DC}	
Gamma Ref. Voltage (Low)	VGML	-0.3	$\frac{1}{2}VDD+0.5$	V _{DC}	
BL Operating Input Voltage (One Side)	VBL	600	1150	V _{RMS}	
Panel Front Temperature	T _{SUR}	-	+68	°C	4
Operating Temperature	T _{OP}	0	+50	°C	2,3
Storage Temperature	T _{ST}	-20	+60	°C	
Operating Ambient Humidity	H _{OP}	10	90	%RH	
Storage Humidity	H _{ST}	10	90	%RH	

Note: 1. Ambient temperature condition ($T_a = 25 \pm 2^\circ\text{C}$)

2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.

3. Gravity mura can be guaranteed below 40 °C condition.

4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.





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3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and GIP.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	V _{DC}	
Logic High Level Input Voltage	V _{IH}		2.7		VCC	V _{DC}	
Logic Low Level Input Voltage	V _{IL}		0		0.6	V _{DC}	
Source D-IC Analog Voltage	VDD	-	15.8	16.0	16.2	V _{DC}	
Half Source D-IC Analog Voltage	H_VDD	-	7.8V +50mV	8.0	8.2V -50mV	V _{DC}	
Gamma Reference Voltage	V _{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V _{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	V _{com}	-	6.26	6.56	6.86	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC≤3.6V			156	MHz	
mini-LVDS input Voltage (Center)	V _{IB}	Mini-LVDS Clock and Data	0.7 + (VID/2)		(VCC-1.2) - VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔV _{IB}				0.8	V	
mini-LVDS differential Voltage range	V _{ID}		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔV _{ID}		25		800	mV	
Gate High Voltage	V _{GH}		26.7 27.7	27.0 28.0	27.3 28.3	V _{DC}	25℃ 0℃
Gate Low Voltage	V _{GL}		-5.2	-5.0	-4.8	V _{DC}	
GIP Bi-Scan Voltage	V _{GI_P} V _{GI_N}	-	V _{GL}	-	V _{GH}	V _{DC}	
GIP Refresh Voltage	V _{GH} even/odd	-	V _{GL}	-	V _{GH}	V	
GIP Start Pulse Voltage	V _{ST}	-	V _{GL}	-	V _{GH}	V	
GIP Operating Clock	GCLK	-	V _{GL}	-	V _{GH}	V	
Total Power Current	I _{LCD}	-		507	660	mA	2
Total Power Consumption	P _{LCD}	-		6.08	7.92	Watt	2

Note: 1. The specified current and power consumption are under the V_{LCD}=12V., 25 ± 2°C, f_V=60Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.

2. The above spec is based on the basic model.

3. All of the typical gate voltage should be controlled within 1% voltage level

4. Ripple voltage level is recommended under 10%

5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.

6. Logic level Input Signal : SOE, POL, GSP, H_CONV, OPT_N

7. HVDD Voltage level is half of VDD and it should be between Gamma9 and Gamma10

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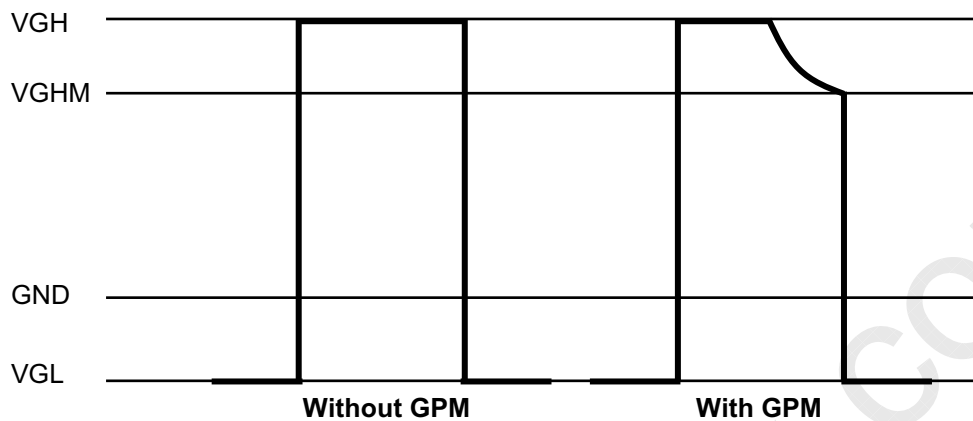
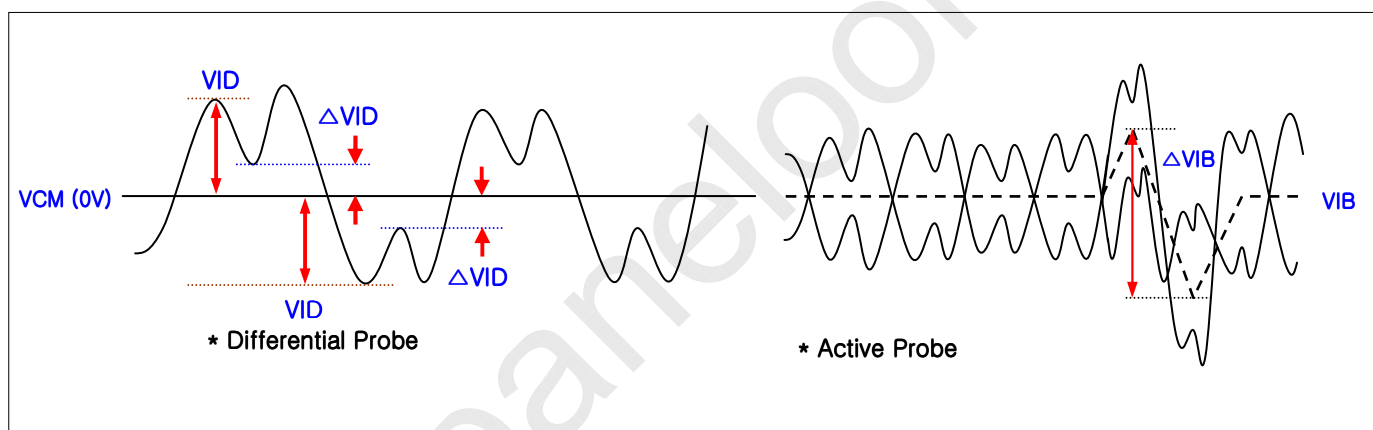


FIG. 1 Gate Output Wave form without GPM and with GPM

FIG. 2 Description of VID, Δ VIB, Δ VID

* Source PCB

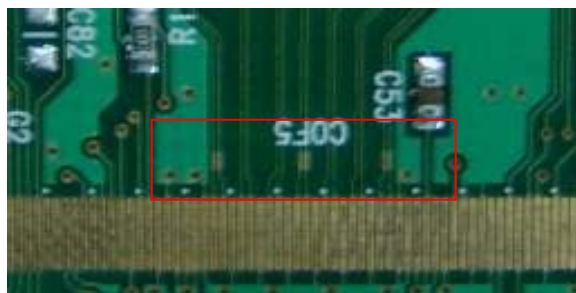


FIG. 3 Measure point

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Table 3. ELECTRICAL CHARACTERISTICS (Continue)

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
Backlight Assembly :						
Operating Voltage (one side,fBL=45KHz, IBL=108mA _{RMS})	VBL		-	24	V	1, 2
Operating Current (one side)	IBL		-	7.5	A	1
Striking Voltage [0℃] (Open Lamp Voltage @ one side)	VOPEN	-	-	1175	V _{RMS}	1, 3
Operating Frequency	fBL	43	45	47	kHz	4
Striking Time	S TIME	1.5	-	-	sec	3
Power Consumption	PBL	-	105	-	Watt	6
Burst Dimming Duty	{a/T} * 100	20		100	%	9
Burst Dimming Frequency	1/T	95		182	Hz	9

Parameter	Symbol	Values			Unit	Note
		Min	Typ	Max		
Lamp : (APPENDIX-V)						
Lamp Voltage (one side)	VLAMP	735	1175	1225	V _{RMS}	1, 2
Lamp Current (one side)	ILAMP	3	7.71	8.21	mA _{RMS}	1
Discharge Stabilization Time	TS	-	-	3	Min	1, 5
Lamp Frequency	f LAMP	43	45	47	KHz	
Established Starting Voltage [0℃]	VS			1175	V _{RMS}	1, 3
Life Time		50,000	60,000		Hrs	7

Note The design of the inverter must have specifications for the lamp in LCD Assembly.

The electrical characteristics of inverter are based on High-High Driving type.

The performance of the lamps in LCM, for example life time or brightness, is extremely influenced by the characteristics of the DC-AC inverter. So, all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

When you design or order the inverter, please make sure unwanted lighting caused by the mismatch of the lamp and the inverter (no lighting, flicker, etc) has never been occurred. When you confirm it, the LCD-Assembly should be operated in the same condition as installed in your instrument.

※ Do not attach a conductive tape to lamp connecting wire.

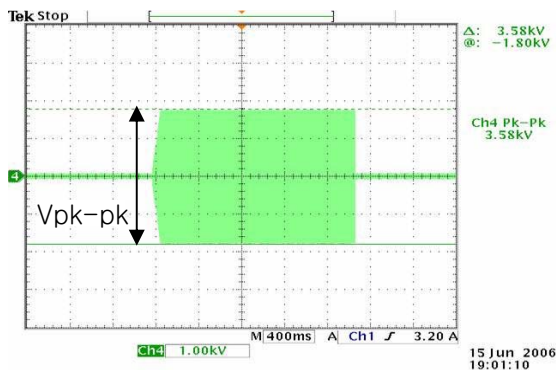
If you attach conductive tape to the lamp wire, not only luminance level can be lower than typical one but also inverter operate abnormally on account of leakage current which is generated between lamp wire and conductive tape.

1. Specified values are defined for a Backlight Assembly.(IBL : 14 lamp, 7.71 mA/Lamp)

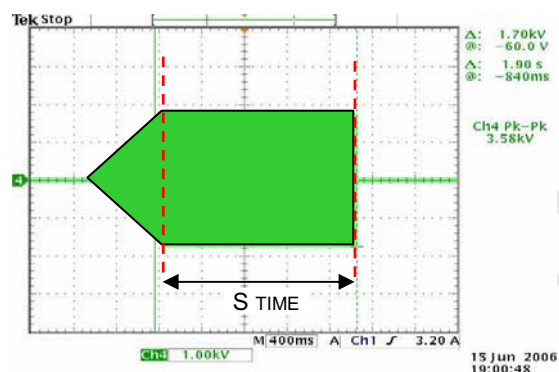
2. Operating voltage is measured at 25 ± 2℃(after 2hr.aging).The variance range for operating voltage is ± 10%.

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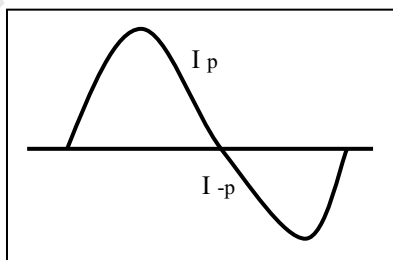
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$$V_s = (V_{pk-pk}) / [2 \cdot \sqrt{2}]$$



3. The Striking Voltage (Open Lamp Voltage) [V_{open}] should be applied to the lamps more than Striking time (S TIME) for start-up. Inverter Striking Voltage must be more than Established Starting Voltage of lamp. Otherwise, the lamps may not be turned on. The used lamp current is typical value.
When the Striking Frequency is higher than the Operating Frequency, the parasitic capacitance can cause inverter shut down, therefore It is recommended to check it.
 4. Lamp frequency may produce interference with horizontal synchronous frequency. As a result this may cause beat on the display. Therefore, lamp frequency shall be away as much as possible from the horizontal synchronous frequency and its harmonics range in order to prevent interference.
There is no reliability problem of lamp, if the operation frequency is typ $\pm 5\text{KHz}$. But it should be applied in less than ABSOLUTE MAXIMUM RATINGS max voltage
 5. The brightness of the lamp after lighted for 5minutes is defined as 100%.
 T_s is the time required for the brightness of the center of the lamp to be not less than 95% at typical current.
The screen of LCD module may be partially dark by the time the brightness of lamp is stable after turn on.
 6. Maximum level of power consumption is measured at initial turn on.
Typical level of power consumption is measured after 2hrs aging at $25 \pm 2^\circ\text{C}$.
 7. The life time is determined as the time at which brightness of the lamp is 50% compared to that of initial value at the typical lamp current on condition of continuous operating at $25 \pm 2^\circ\text{C}$, based on duty 100%.
 8. The output of the inverter must have symmetrical (negative and positive) voltage and current waveform (Unsymmetrical ratio is less than 10%). Please do not use the inverter which has not only unsymmetrical voltage and current but also spike wave.
Requirements for a system inverter design, which is intended to achieve better display performance, power efficiency and more reliable lamp characteristics.
It can help increase the lamp lifetime and reduce leakage current.
 - a. The asymmetry rate of the inverter waveform should be less than 10%.
 - b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$.
- * Inverter output waveform had better be more similar to ideal sine wave.



* Asymmetry rate:

$$|I_p - I_{-p}| / I_{oRMS} \times 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{oRMS}$$

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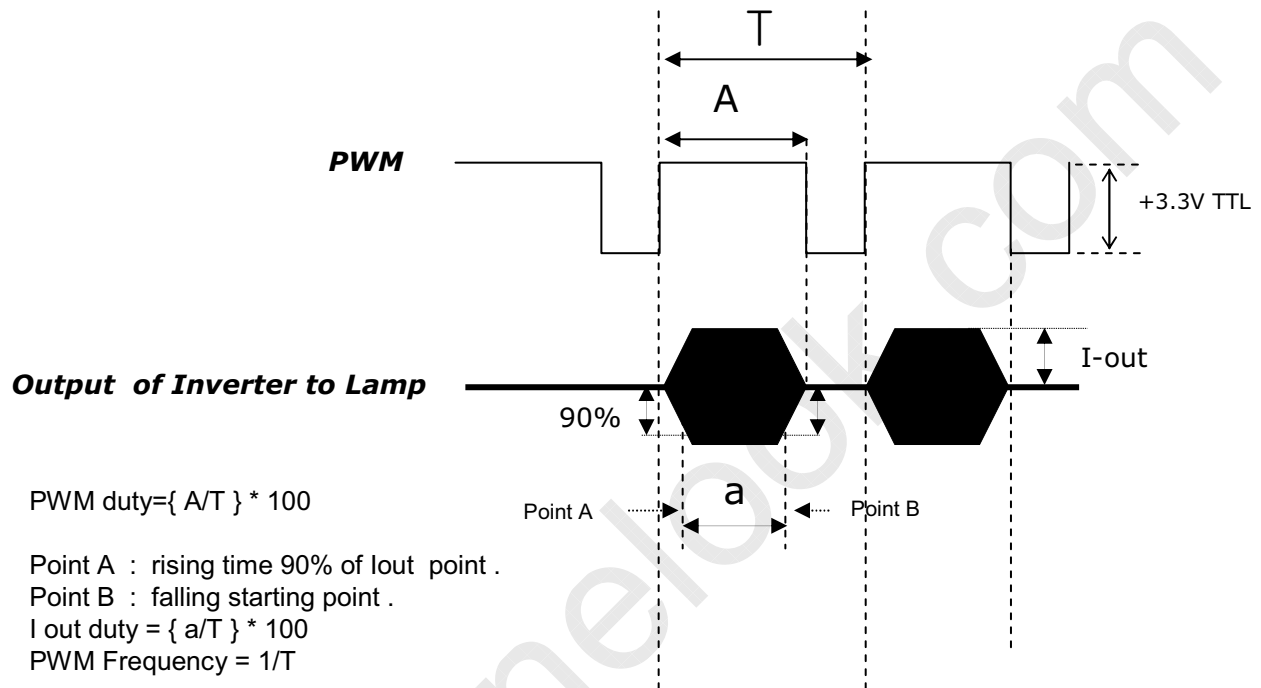
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9. The reference method of burst dimming duty ratio.

It is recommended to use synchronous V-sync frequency to prevent waterfall

(Vsync $\times 2$ =Burst Frequency)

Though PWM frequency is over 182Hz (max252Hz), function of backlight is not affected.



※ We recommend not to be much different between PWM duty and Iout duty .

※ Dimming current output rising and falling time may produce humming and inverter trans' sound noise.

※ Burst dimming duty should be 100% for more than 1second after turn on.

※ Equipment

Oscilloscope :TDS3054B(Tektronix)

Current Probe : P6022 AC (Tektronix)

High Voltage Probe: P5100(Tektronix)

10. The Cable between the backlight connector and its inverter power supply should be connected directly with a minimized length. The longer cable between the backlight and the inverter may cause the lower luminance of lamp and may require more higher starting voltage (Vs).

11. The operating current must be measured as near as backlight assembly input.

12. The operating current unbalance between left and right must be under 10% of Typical current
 | Left(Master) current – Right(Slave) Current | < 10% of typical current



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3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 60-pin FFC connector are used for the module electronics and two 3-pin Balance PCB connectors are used for the integral backlight system.

3-2-1. LCD Module

-LCD Connector (CN1): TF06L-60S-0.5SH (Manufactured by HRS) or Equivalent

Table 4-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	31	LLV3 -	Left Mini LVDS Receiver Signal(3-)
2	LTD_OUT	LTD OUTPUT	32	LLV3 +	Left Mini LVDS Receiver Signal(3+)
3	GCLK1	GIP GATE Clock 1	33	LCLK -	Left Mini LVDS Receiver Clock Signal(-)
4	GCLK2	GIP GATE Clock 2	34	LCLK +	Left Mini LVDS Receiver Clock Signal(+)
5	GCLK3	GIP GATE Clock 3	35	LLV2 -	Left Mini LVDS Receiver Signal(2-)
6	GCLK4	GIP GATE Clock 4	36	LLV2 +	Left Mini LVDS Receiver Signal(2+)
7	GCLK5	GIP GATE Clock 5	37	LLV1 -	Left Mini LVDS Receiver Signal(1-)
8	GCLK6	GIP GATE Clock 6	38	LLV1 +	Left Mini LVDS Receiver Signal(1+)
9	VGI_N	GIP Bi-Scan (Normal =VGL)	39	LLV0 -	Left Mini LVDS Receiver Signal(0-)
10	VGI_P	GIP Bi-Scan (Normal =VGH)	40	LLV0 +	Left Mini LVDS Receiver Signal(0+)
11	VGH_ODD	GIP Panel VDD for Odd GATE TFT	41	GND	Ground
12	VGH_EVEN	GIP Panel VDD for Even GATE TFT	42	SOE	Source Output Enable SIGNAL
13	VGL	GATE Low Voltage	43	POL	Polarity Control Signal
14	VST	VERTICAL START PULSE	44	GSP	GATE Start Pulse
15	GND	Ground	45	H_CONV	"H" H 2dot Inversion/ "L" H 1dot Inversion
16	VCOM_L_FB	VCOM Left Feed-Back Output	46	OPT_N	"H" Normal Display
17	VCOM_L	VCOM Left Input	47	GND	Ground
18	GND	Ground	48	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)
19	VDD	Driver Power Supply Voltage	49	GMA 16	GAMMA VOLTAGE 16
20	VDD	Driver Power Supply Voltage	50	GMA 15	GAMMA VOLTAGE 15
21	H_VDD	Half Driver Power Supply Voltage	51	GMA 14	GAMMA VOLTAGE 14
22	H_VDD	Half Driver Power Supply Voltage	52	GMA 12	GAMMA VOLTAGE 12
23	GND	Ground	53	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)
24	VCC	Logic Power Supply Voltage	54	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)
25	VCC	Logic Power Supply Voltage	55	GMA 7	GAMMA VOLTAGE 7
26	GND	Ground	56	GMA 5	GAMMA VOLTAGE 5
27	LLV5 -	Left Mini LVDS Receiver Signal(5-)	57	GMA 4	GAMMA VOLTAGE 4
28	LLV5 +	Left Mini LVDS Receiver Signal(5+)	58	GMA 3	GAMMA VOLTAGE 3
29	LLV4 -	Left Mini LVDS Receiver Signal(4-)	59	GMA 1	GAMMA VOLTAGE 1(Output From LCD)
30	LLV4 +	Left Mini LVDS Receiver Signal(4+)	60	GND	Ground

Note : 1. Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.
2. These 'input signal' (OPT_N,H_CONV) should be connected



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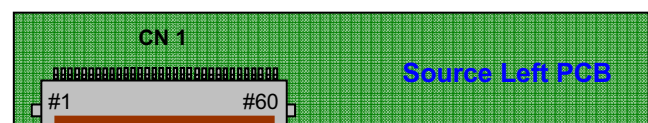
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-LCD Connector (CN2): TF06L-60S-0.5SH(Manufactured by HRS) or Equivalent

Table 4-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	31	RLV1 -	Right Mini LVDS Receiver Signal(1-)
2	GMA 1	GAMMA VOLTAGE 1 (Output From LCD)	32	RLV1 +	Right Mini LVDS Receiver Signal(1+)
3	GMA 3	GAMMA VOLTAGE 3	33	RLV0 -	Right Mini LVDS Receiver Signal(0-)
4	GMA 4	GAMMA VOLTAGE 4	34	RLV0 +	Right Mini LVDS Receiver Signal(0+)
5	GMA 5	GAMMA VOLTAGE 5	35	GND	Ground
6	GMA 7	GAMMA VOLTAGE 7	36	VCC	Logic Power Supply Voltage
7	GMA 9	GAMMA VOLTAGE 9 (Output From LCD)	37	VCC	Logic Power Supply Voltage
8	GMA 10	GAMMA VOLTAGE 10 (Output From LCD)	38	GND	Ground
9	GMA 12	GAMMA VOLTAGE 12	39	H_VDD	Half Driver Power Supply Voltage
10	GMA 14	GAMMA VOLTAGE 14	40	H_VDD	Half Driver Power Supply Voltage
11	GMA 15	GAMMA VOLTAGE 15	41	VDD	Driver Power Supply Voltage
12	GMA 16	GAMMA VOLTAGE 16	42	VDD	Driver Power Supply Voltage
13	GMA 18	GAMMA VOLTAGE 18 (Output From LCD)	43	GND	Ground
14	GND	Ground	44	VCOM_R	VCOM Right Input
15	OPT_N	"H" Normal Display	45	VCOM_R_FB	VCOM Right Feed-Back Output
16	H_CONV	"H" H 2dot Inversion/ "L" H 1dot Inversion	46	GND	Ground
17	GSP	GATE Start Pulse	47	VST	VERTICAL START PULSE
18	POL	Polarity Control Signal	48	VGL	GATE Low Voltage
19	SOE	Source Output Enable SIGNAL	49	VGH_EVEN	GIP Panel VDD for Even GATE TFT
20	GND	Ground	50	VGH_ODD	GIP Panel VDD for Odd GATE TFT
21	RLV5 -	Right Mini LVDS Receiver Signal(5-)	51	VGI_P	GIP Bi-Scan (Normal =VGH)
22	RLV5 +	Right Mini LVDS Receiver Signal(5+)	52	VGI_N	GIP Bi-Scan (Normal =VGL)
23	RLV4 -	Right Mini LVDS Receiver Signal(4-)	53	GCLK6	GIP GATE Clock 6
24	RLV4 +	Right Mini LVDS Receiver Signal(4+)	54	GCLK5	GIP GATE Clock 5
25	RLV3 -	Right Mini LVDS Receiver Signal(3-)	55	GCLK4	GIP GATE Clock 4
26	RLV3 +	Right Mini LVDS Receiver Signal(3+)	56	GCLK3	GIP GATE Clock 3
27	LCLK -	Right Mini LVDS Receiver Clock Signal(-)	57	GCLK2	GIP GATE Clock 2
28	LCLK +	Right Mini LVDS Receiver Clock Signal(+)	58	GCLK1	GIP GATE Clock 1
29	RLV2 -	Right Mini LVDS Receiver Signal(2-)	59	LTD_OUT	LTD OUTPUT
30	RLV2 +	Right Mini LVDS Receiver Signal(2+)	60	GND	Ground

Note : 1.Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.
2. These 'input signal' (OPT_N,H_CONV) should be connected



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3-2-2. Backlight Module

[Master]

1) Balance Connector

: 65002WS-03 (manufactured by YEONHO) or equivalent

2) Mating Connector

: 65002HS-03 (manufactured by YEONHO) or equivalent.

[Slave]

1) Balance Connector

: 65002WS-03 (manufactured by YEONHO) or equivalent

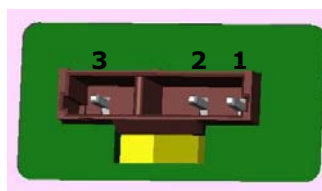
2) Mating Connector

: 65002HS-03 (manufactured by YEONHO) or equivalent.

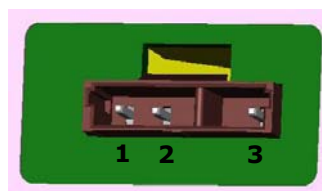
Table 5. BACKLIGHT CONNECTOR PIN CONFIGURATION(CN3,CN4)

No	Symbol	Master	Slave	Note
1	H_Input	High_Input	High_Input	
2	H_Input	High_Input	High_Input	
3	FB	NC	NC	

◆ Rear view of LCM



Master



Slave



[Master]



[Slave]

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3-3. Signal Timing Specifications

Table 6. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T1		6.4	6.7		ns	1
Mini Clock pulse low period	T2		3.2	-	-	ns	
Mini Clock pulse high period	T3		3.2	-	-	ns	
Mini Data setup time	T6		1.2	-	-	ns	
Mini Data hold time	T7		1.2	-	-	ns	
Reset low to SOE rising time	T8		0	-	-	ns	
SOE to Reset input time	T9		200	-	-	ns	
Receiver off to SOE timing	T10		10	-	-	CLK cycle	
POL signal to SOE setup time	T11		-5	-	-	ns	
POL signal to SOE hold time	T12		6	-	-	ns	
Reset High Period	T13		3			CLK cycle	
SOE signal GSP setup time	T14		100			ns	
SOE signal GSP Hold time	T15		100			ns	
SOE signal Pulse Width	T16		200			ns	

- Note : 1. mini-LVDS timing measure conditions:
: 126 MHz < Clock Frequency < 156 MHz , 150mV < VID < 800mV @ 3.0 < VCC < 3.3
2. Setup time and hold time should be satisfied at the same time

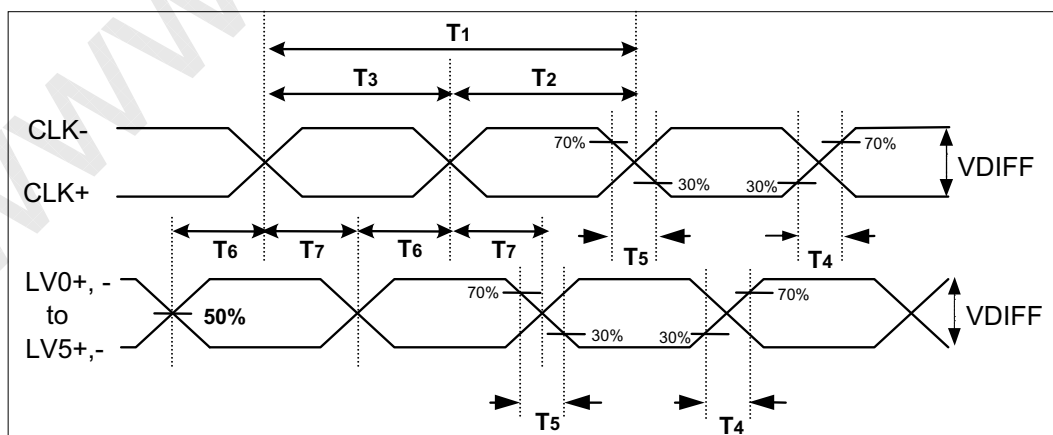


FIG 4. Source D-IC Input Data Latch Timing Waveform

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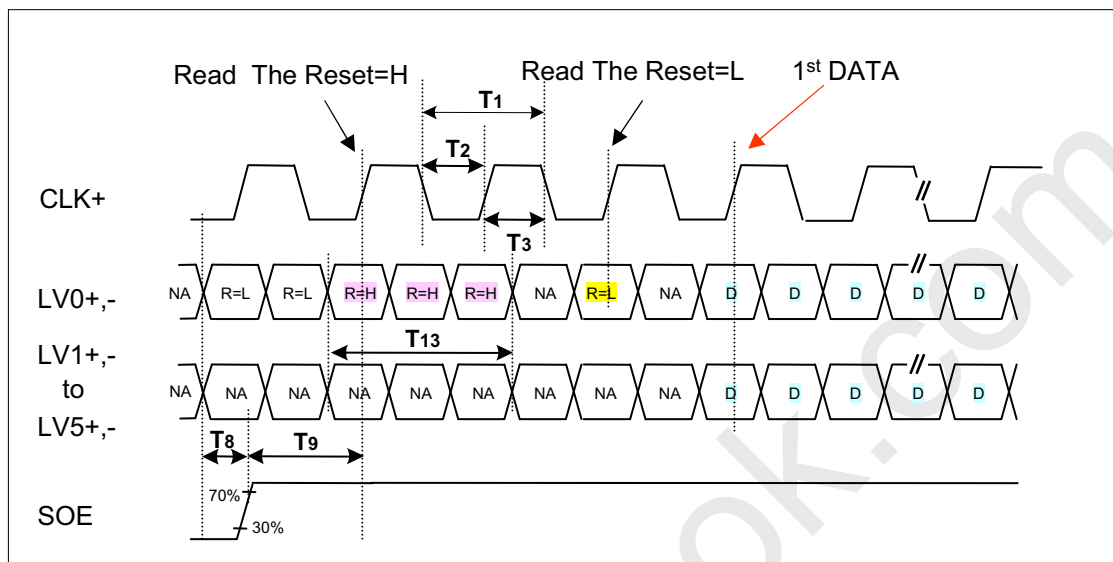
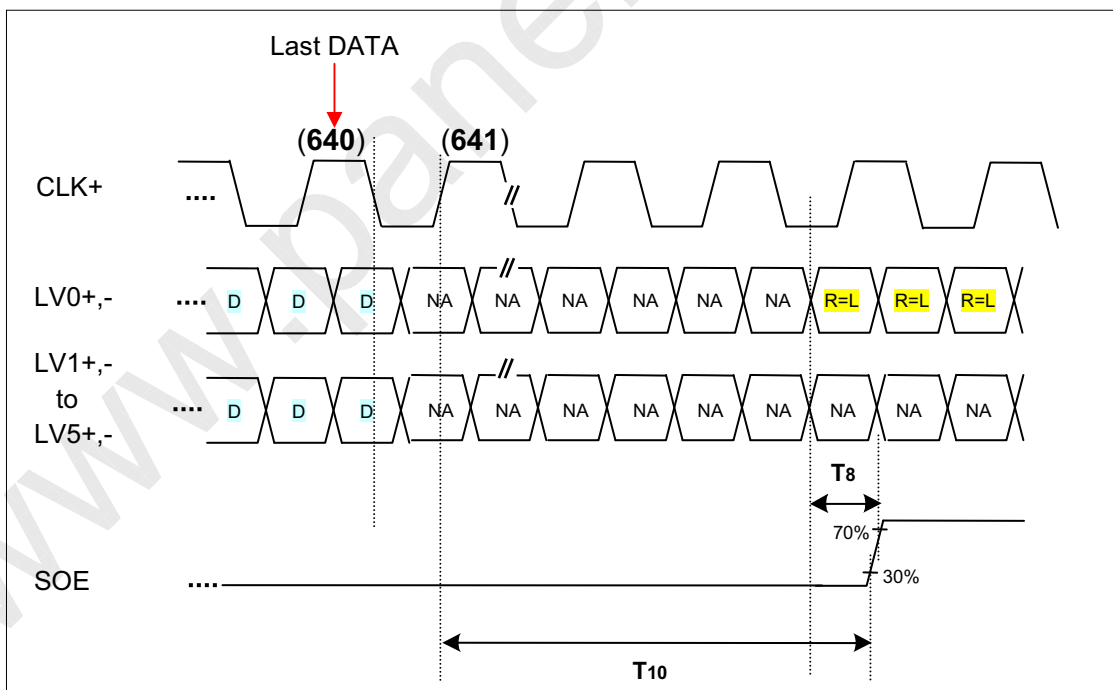
FIG 5-1. Input Data Timing for 1st Source D-IC Chip

FIG 5-2. Last Data Latch to SOE Timing

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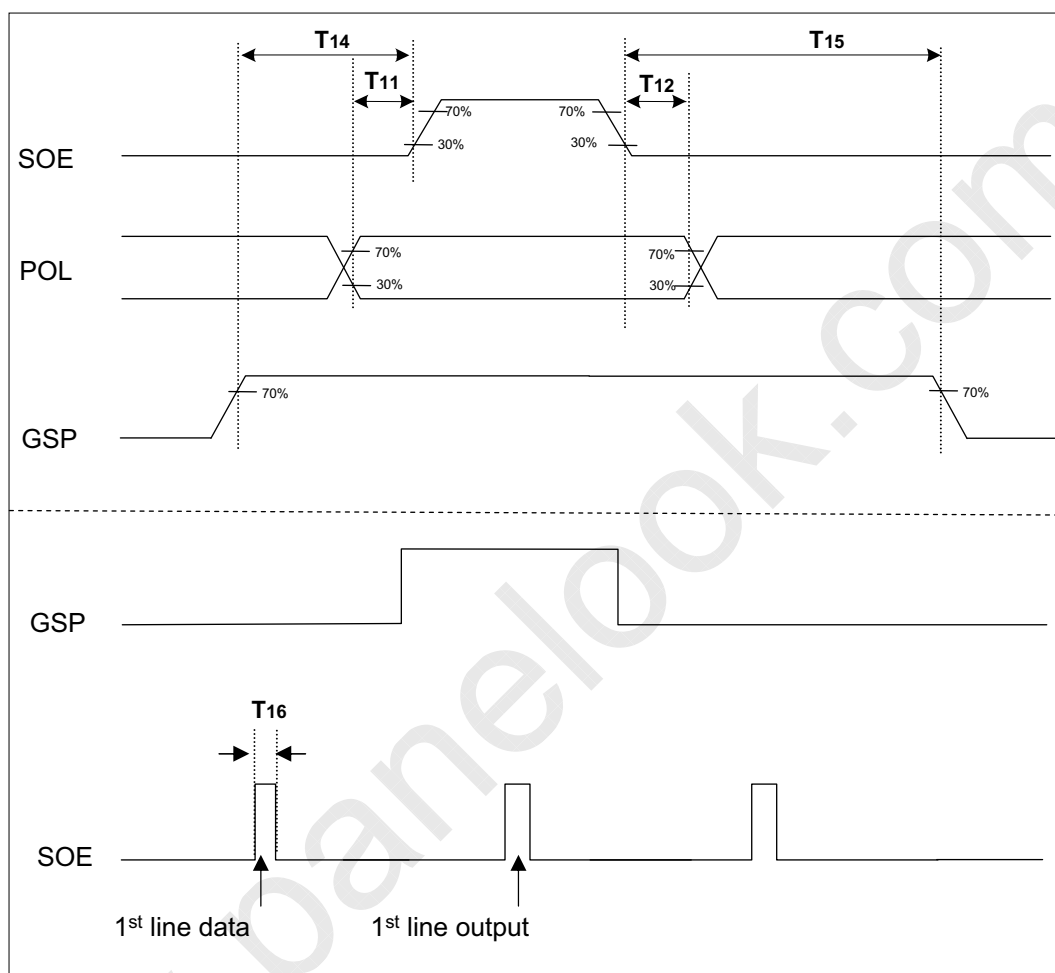


FIG 6. POL, GSP and SOE Timing Waveform

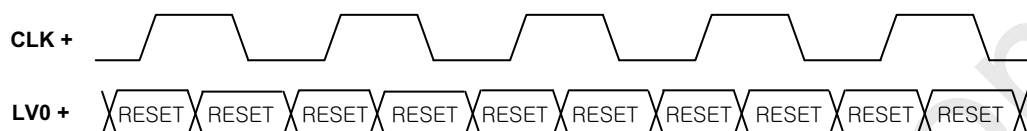
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3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

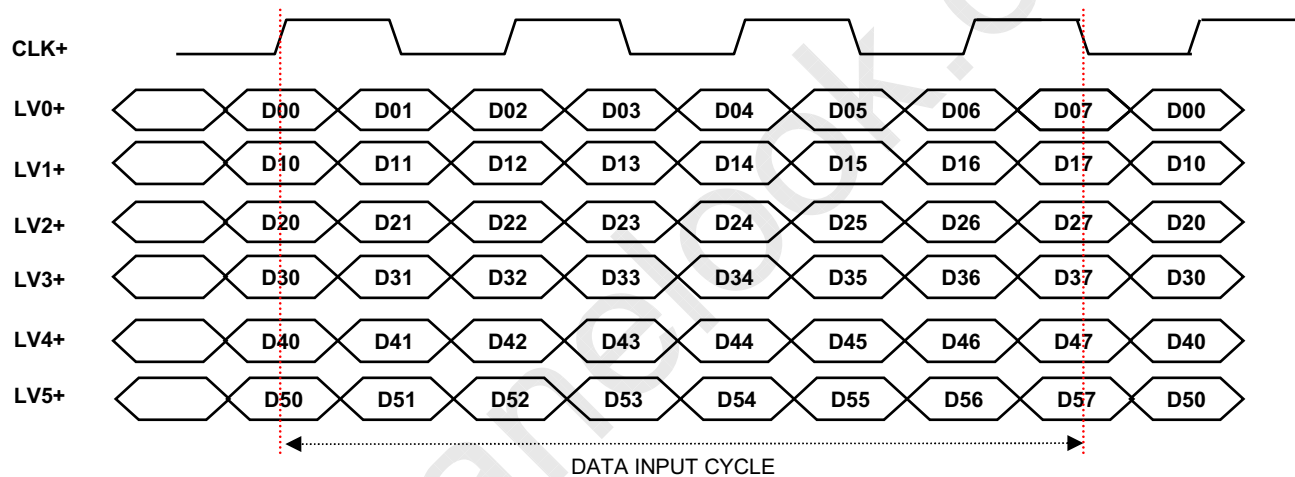


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

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3-5. Panel Pixel Structure

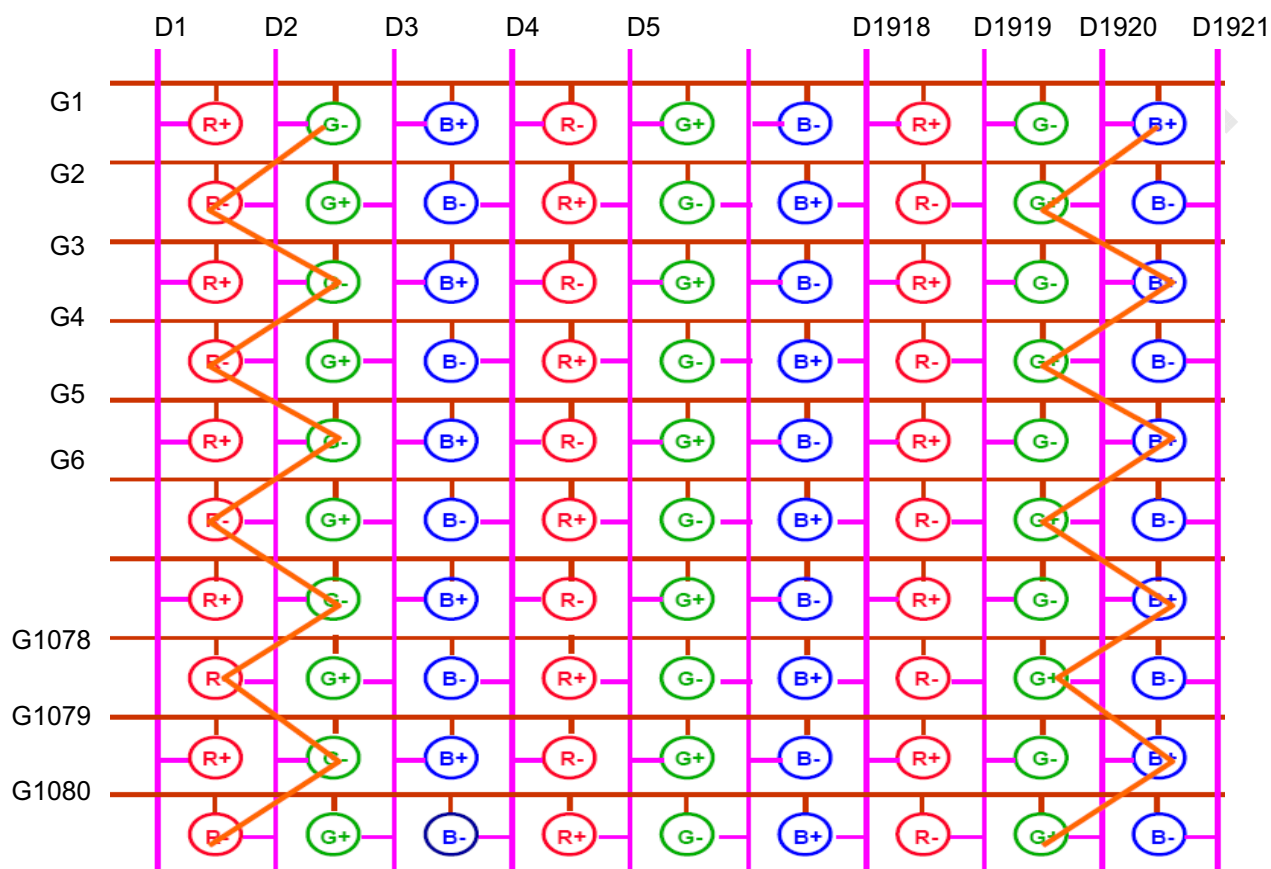


FIG. 8 Panel Pixel Structure

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3-6. Power Sequence

3-6-1. LCD Driving circuit

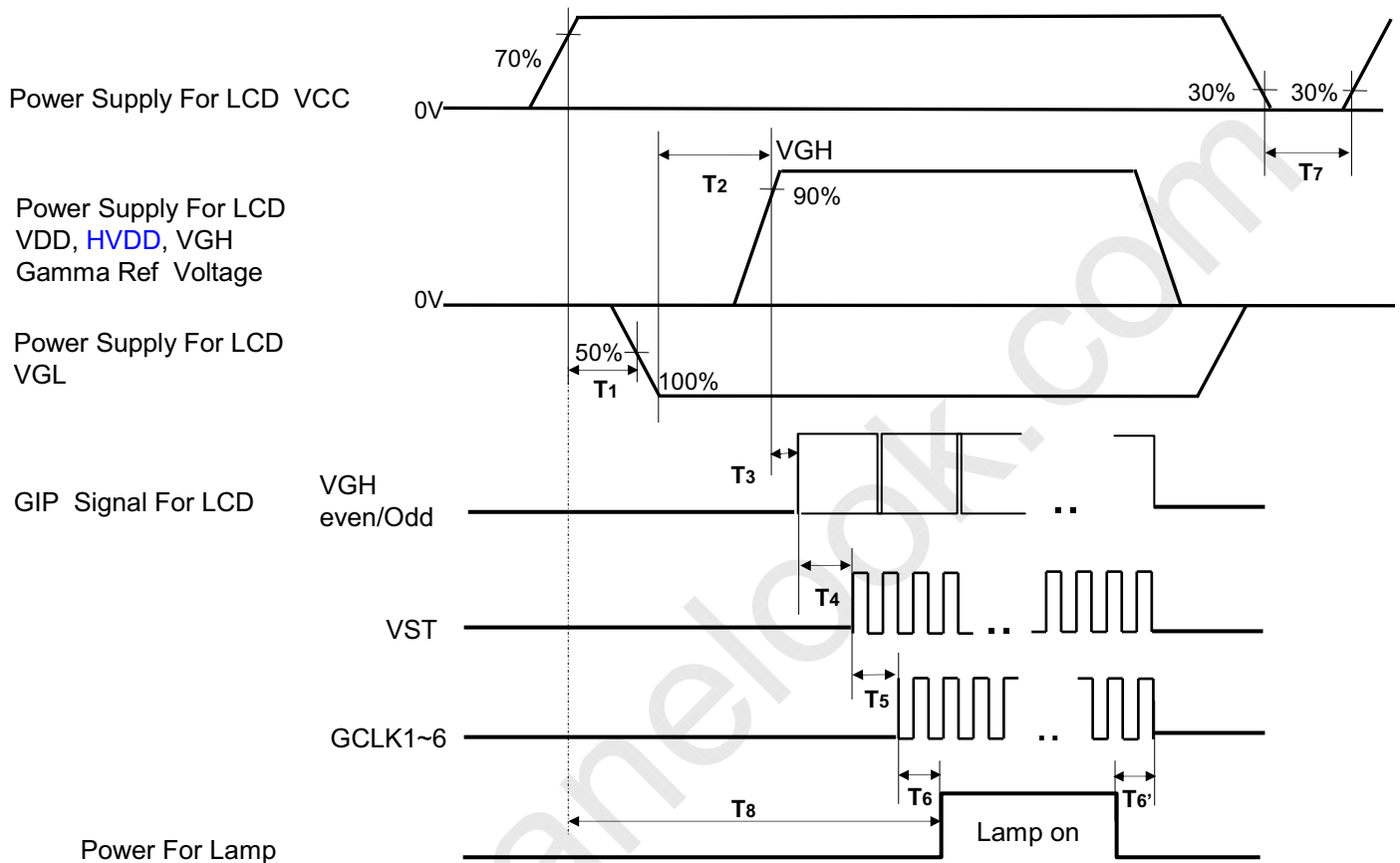


Table 7. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.5		-	ms	
T3	0		-	ms	
T4	10		-	ms	2
T5	0		-	ms	
T6 / T6'	20		-	ms	
T7	2		-	s	
T8	-		12	s	

- Note :
1. Power sequence for Source D-IC must be kept. ※ Please refer to Appendix IV-1 for more details.
 2. VGH Odd signal should be started "High" status and VGH even & odd can not be "High at the same time.
 3. Power Off Sequence order is reverse of Power On Condition including Source D-IC.
 4. GCLK On/Off Sequence : GCLK4 → GCLK5 → GCLK6 → GCLK1 → GCLK2 → GCLK3.
 5. VDD Odd/Even transition time should be within V blank

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4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at $25\pm 2^{\circ}\text{C}$. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0° .

It is presented additional information concerning the measurement equipment and method in FIG. 9.

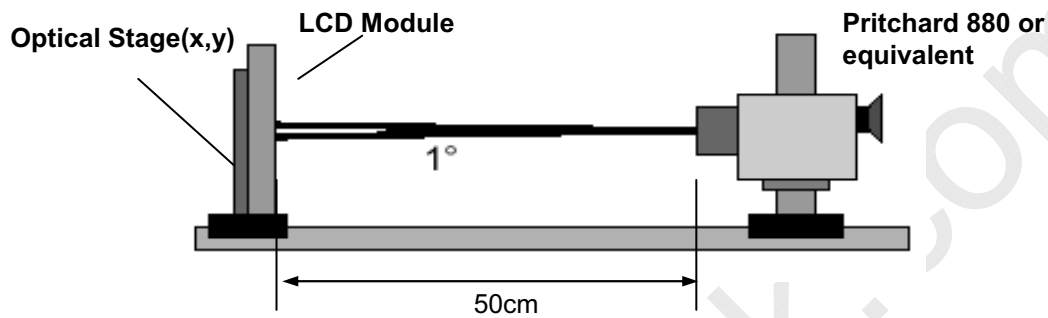


FIG. 9 Optical Characteristic Measurement Equipment and Method

$T_a = 25\pm 2^{\circ}\text{C}$, VDD, H_VDD, VGH, VGL=typ,

fV= 60Hz, Clk=148.5MHz, $I_{BL}=108\text{ mA}_{RMS}$, Iout duty = 100%

Table 8. OPTICAL CHARACTERISTICS

Parameter		Symbol		Value			Unit	Note
				Min	Typ	Max		
Contrast Ratio		CR		1000	1500	-		1
Surface Luminance, white		L _{WH}		-	-	1500	nit	2
Luminance Variation		δ _{WHITE}	5P	-	-	1.3		3
Response Time	Rising	Tr		-	8	12	ms	4
	Falling	Tf		-	10	14		
Color Coordinates [CIE1931]	RED	Rx		Typ -0.03	0.642	Typ +0.03		
		Ry			0.334			
	GREEN	Gx			0.292			
		Gy			0.607			
	BLUE	Bx			0.146			
		By			0.056			
	WHITE	Wx			0.279			
		Wy			0.292			
Color Temperature					10,000		K	
Color Gamut					72		%	
Viewing Angle (CR>10)								
	x axis, right(φ=0°)	θr		89	-	-	degree	5
	x axis, left (φ=180°)	θl		89	-	-		
	y axis, up (φ=90°)	θu		89	-	-		
	y axis, down (φ=270°)	θd		89	-	-		
Gray Scale				-	-	-		6

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Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at $25 \pm 2^\circ\text{C}$. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 10.

3. The variation in surface luminance, δ WHITE is defined as :

$$\delta \text{ WHITE}(5P) = \text{Maximum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5}) / \text{Minimum}(L_{on1}, L_{on2}, L_{on3}, L_{on4}, L_{on5})$$

Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .

For more information, see the FIG. 10.

4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D).

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

6. Gray scale specification

Gamma Value is approximately 2.2. For more information, see the Table 9.

Table 9. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.07
L15	0.27
L31	1.04
L47	2.49
L63	4.68
L79	7.66
L95	11.5
L111	16.1
L127	21.6
L143	28.1
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L1	Gamma8
	L31	Gamma7
	L63	Gamma6
	L127	Gamma5
	L191	Gamma4
	L223	Gamma3
	L255	Gamma1
Negative Voltage	L255	Gamma18
	L223	Gamma16
	L191	Gamma15
	L127	Gamma14
	L63	Gamma13
	L31	Gamma12
	L1	Gamma11
	L0	Gamma10

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Measuring point for surface luminance & luminance variation

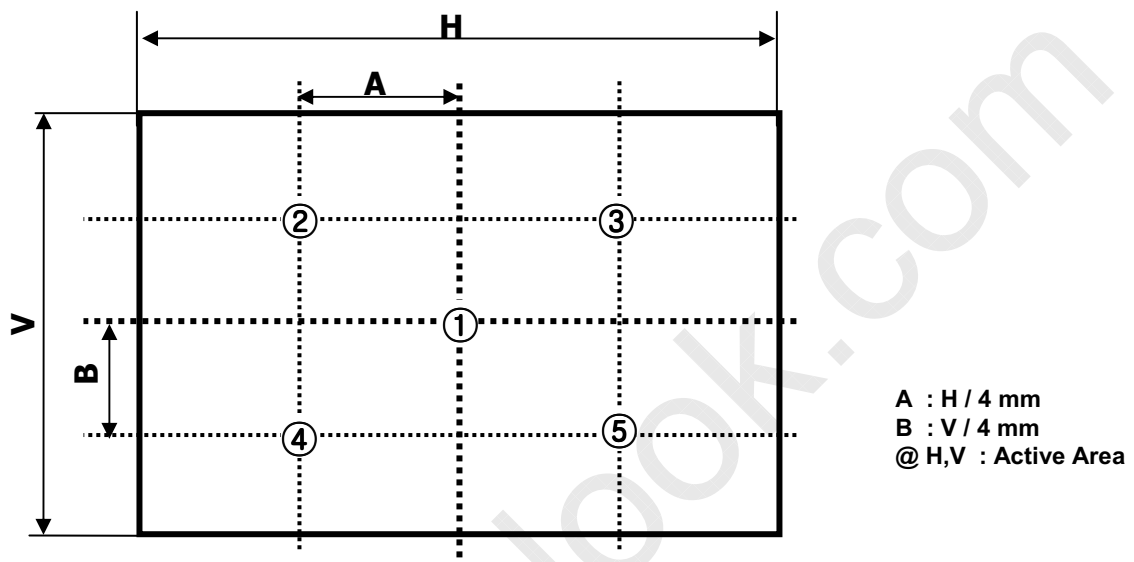


FIG. 10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

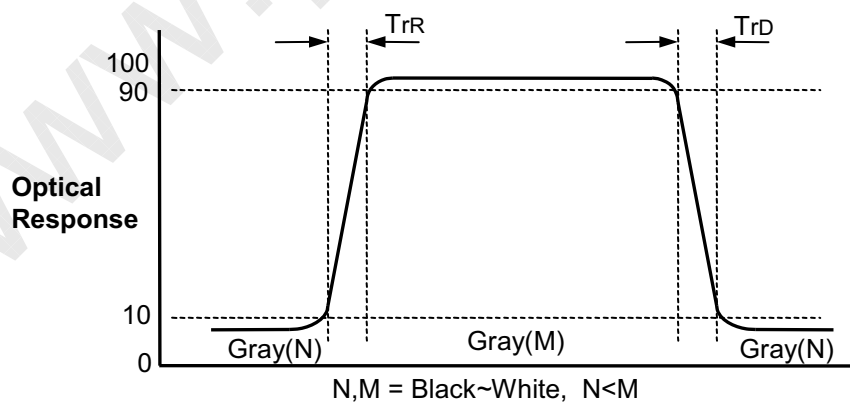


FIG. 11 Response Time

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Dimension of viewing angle range

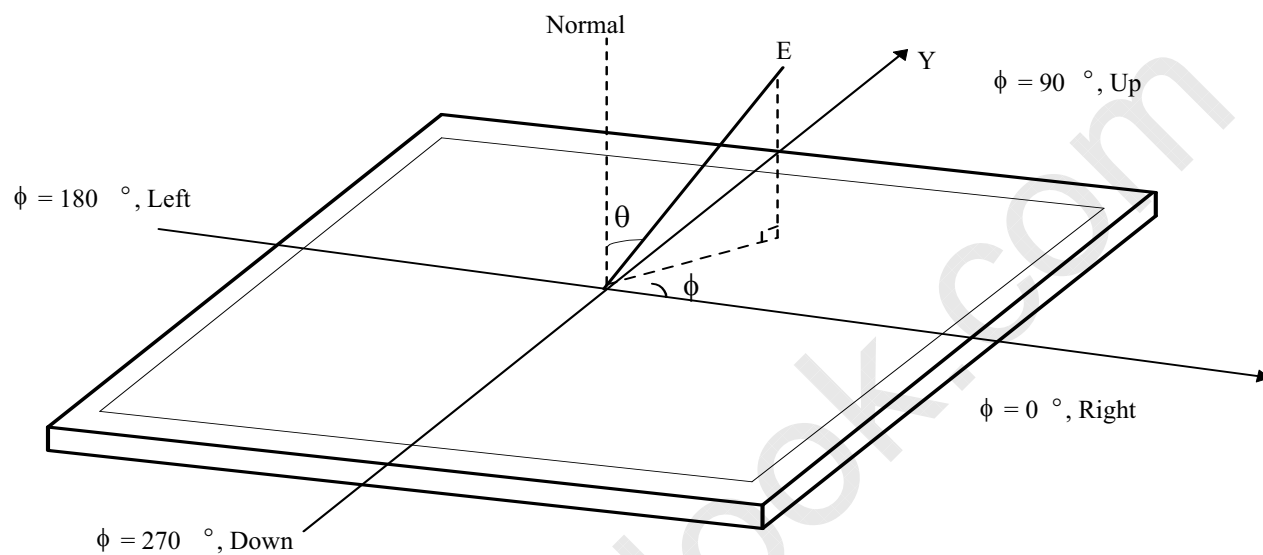


FIG.12 Viewing Angle



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5. Mechanical Characteristics

Table 10 provides general mechanical characteristics.

Table 10. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	760.0 mm
	Vertical	450.0 mm
	Depth	32.5 mm
Bezel Area	Horizontal	703.8 mm
	Vertical	398.4 mm
Active Display Area	Horizontal	698.4 mm
	Vertical	392.85 mm
Weight	5.0 Kg (Typ.) , 5.5Kg (Max.)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

Product Specification

[FRONT VIEW]

